Exhibit 16

UNITED STATES DISTRICT COURT
FOR THE WESTERN DISTRICT OF TEXAS
WACO DIVISION

SOLAS OLED LTD., *Plaintiff,* v. LG DISPLAY CO., LTD., LG ELECTRONICS, INC., and SONY CORPORATION, *Defendants.*	Case No. 6:19-cv-00236-ADA

DECLARATION OF RICHARD A. FLASCK IN SUPPORT OF SOLAS'S RESPONSIVE CLAIM CONSTRUCTION BRIEF

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TABLE OF EXHIBITS AND ABBREVIATIONS

Ex [1]	Document Description	Abbreviation
1	Declaration of Richard A. Flasck in support of Solas's opening claim construction brief	Flasck. Decl.
2	U.S. Patent No. 7,907,137	'137 patent
3	U.S. Patent No. 7,432,891	'891 patent
4	U.S. Patent No. 7,573,068	'068 patent
5	Parties' joint revised list of terms/constructions dated March 6, 2020	Joint Chart
6	Microsoft Computer Dictionary (3rd ed., 1997), definition of "signal"	MS Dict.
7	McGraw-Hill Dictionary of Scientific and Technical Terms (4th ed., 1989), definition of "data transmission line"	McGraw-Hill
8	Merriam-Webster Dictionary (avail. at www.merriam-webster.com, accessed Feb 2020), definitions of "along" and "together"	Merriam-Webster
9	Dictionary.com (avail. at www.dictionary.com, accessed Feb. 2020), definitions of "along" and "together"	Dictionary.com
10	Defendant LG Display's petition for *inter partes* review in IPR2020-00177 on the '891 patent	'891 IPR Pet.
11	Defendant LG Display's expert declaration by Dr. Hatalis in *inter partes review* in IPR2020-00177 on the '891 patent	'891 IPR Decl.
12	U.S. Patent No. 5,106,652	'652 patent
13	U.S. Patent No. 5,981,317	'317 patent
14	U.S. Patent Appl. Pub. No. 2002/0101172	'173 app. pub.
15	U.S. Patent No. 7,250,722	'722 patent
	Declaration of Douglas R. Holberg in support of Defendants' opening claim construction brief (Dkt. 67-2)	Holberg Decl.

[1] Exhibits 1–15 submitted with Solas's opening claim construction brief (Dkt. 68-2 to 68-16)

I. AGREED TERMS

1. I understand that Solas and Defendants LG Display Co., LTD., LG Electronics, Inc., and Sony Corporation (collectively, "Defendants") have agreed to the following constructions:

- "luminance gradation" ('137 patent claims 10, 36) means "light emitting level"
- "supply lines" ('068 patent claims 1, 13) means "conductive lines supplying current or voltage"

II. DISPUTED TERMS FOR '137 PATENT

A. "a gradation current having a current value" ('137 patent claims 10, 36)

Solas's Proposed Construction	Defendants' Proposed Construction
"gradation current" means "current conveying information about a level"; thus, the full construction is a current having a current value and conveying information about a level	an actual current (not voltage) with a value corresponding to a luminance level

2. As Dr. Holberg acknowledges, currents and voltages are related to one another and occur together in electronic circuits. Indeed, due to Ohm's Law, current is proportional to voltage in resistive circuits. In circuits comprising non-linear circuit elements, such as diodes and transistors, the relationship between voltage and current is more complex than Ohm's Law. Dr. Holberg is correct that configurations can exist (the unconnected battery is Dr. Holberg's example) where a voltage can exist yet no current flows. However, he fails to mention at this point that any level of current, large or small, in an electronic circuit requires a voltage. In fact, from a very fundamental perspective, the voltage causes a current. Dr. Holberg admits this in para 26: "'Voltage' is the potential energy required to move electrons from one point to another in a circuit. Ex. 2 at (IEEE

100) at 1260." Electrons have a charge and move, creating a current, when they experience an electric field (experience a voltage).

3. Voltage is the causal agent; current is the result. A current or current signal is caused by a voltage or voltage signal. Voltage can exist even at a time when no current is flowing. But current cannot exist without a voltage. Any current, including any gradation current, is accompanied by or associated with a voltage.

4. Using Dr. Holberg's water analogy: When watering the garden with a garden hose connected to the house spigot, a) the higher the water pressure (voltage) at the house, the more gallons per minute (current) is delivered by the hose, b) if the hose kinks (the resistance in Ohm's Law becomes infinite), flow stops even though the spigot is providing water pressure; we have voltage without current. However, if the water pressure (voltage) at the house goes to zero (maybe the water company has turned off your water to make pipe repairs in the street), the hose flow (current) goes to zero. There is no way there can be a hose flow (current) without water pressure (voltage). Further, if the house water pressure is intentionally varied up and down, we have a pressure (voltage) signal. The resulting variation in hose flow is a flow (current) signal. It is the variation in pressure (voltage) that regulates flow (current). There is no current signal without a causal voltage signal.

5. The description of the invention in the patent shows that the gradation current is related to voltages. The gradation current is generated within the gradation signal generation unit from a voltage using a "voltage-current converter." (10:45–11:3.) This current supplies the electric charges that charge the capacitor with "the voltage component Vdata appropriately corresponding to the gradation signal (display data)," providing a "current/voltage conversion function." (22:37–

54, 24:38–39.) The result of this process is a "gradation voltage" that is applied to the gate of the drive transistor. (2:49–52, 11:4–13.)

6. Ultimately, the gradation current signal used to program the pixel is caused by a voltage signal. It is this voltage component that ultimately is captured on the gate of the drive transistor, determining the current flowing from source to drain of the drive transistor. To have the correct current flowing through the drive transistor and the OLED, the correct voltage (not current) must be present on the gate of the drive transistor. The gradation current allows a voltage to be added to the gate of the drive transistor.

7. With the water analogy in mind: Currents (flow) and voltages (pressure) are inter-related (see Holberg declaration para 27). Current (flow) is caused by voltage (pressure). The gradation current is caused by voltage provided by the off-pixel circuitry. By forcing the gradation current through the pixel circuitry, a voltage (a portion of the total voltage supplied by the off-pixel circuitry) appears on the gate of the drive transistor. That voltage from the gradation current is added to the threshold voltage provided during the pre-charge period. The sum of these two voltages reside on the drive transistor gate during the OLED emission period to allow the correct current to flow though the drive transistor and the OLED to emit the correct amount of light. ('137 col 22:60-64) In essence, the gradation current is one method of adding a voltage to the drive transistor gate. A POSITA would easily understand this.

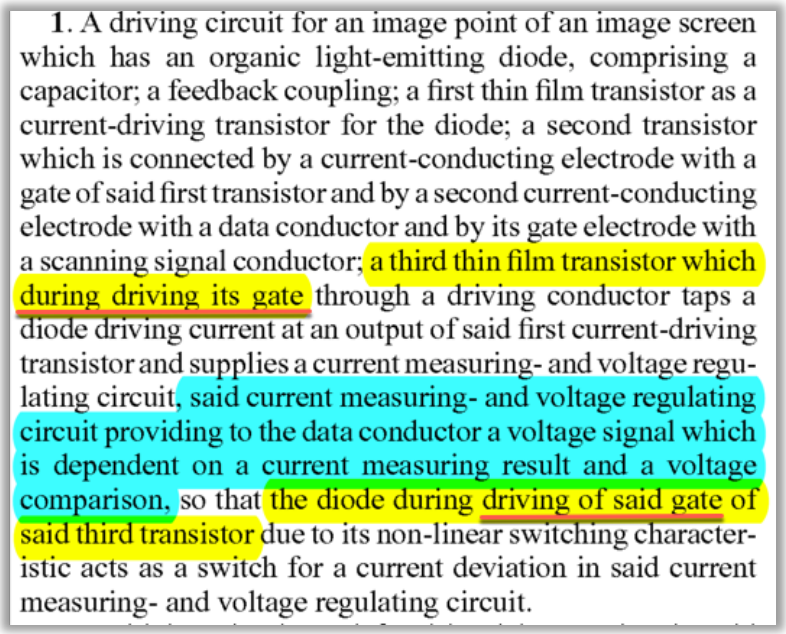
8. For these reasons, a POSITA would understand that a gradation current inevitably is caused by and in turn causes voltages. A POSITA would understand that the claims cover gradation currents that are associated with voltages and do not require that no voltages be present.

III. DISPUTED TERMS FOR '891 PATENT

A. "a third thin film transistor which during driving its gate through a driving conductor taps a diode driving current at an output of said first current-driving transistor and supplies a current measuring- and voltage regulating circuit, said current measuring- and voltage regulating circuit providing to the data conductor a voltage signal which is dependent on a current measuring result and a voltage comparison" ('891 patent claims 1, 3)

Solas's Proposed Construction	Defendants' Proposed Construction
Plain and ordinary meaning. The claimed "providing" by the current measuring- and voltage regulating circuit ("said current measuring- and voltage regulating circuit providing to the data conductor a voltage signal which is dependent on a current measuring result and a voltage comparison") is not required to occur during driving of the third thin film transistor's gate.	The claimed "providing" by the current measuring- and voltage regulating circuit ("said current measuring- and voltage regulating circuit providing to the data conductor a voltage signal which is dependent on a current measuring result and a voltage comparison") is required to occur during driving of the third thin film transistor's gate.

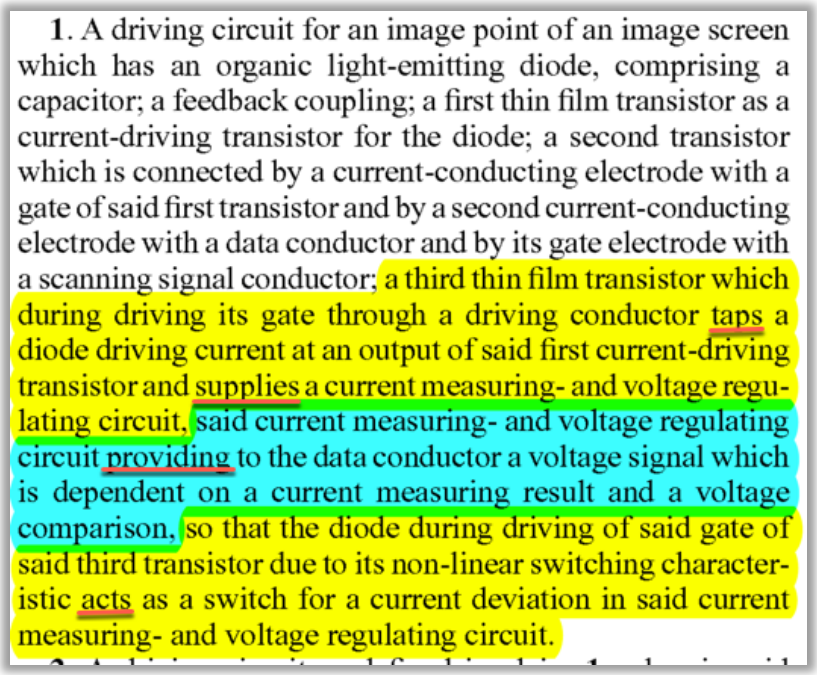
9. Dr. Holberg does asserts that the claim language requires the claimed "providing" by the current measuring- and voltage regulating (CMVR) circuit to occur during driving of the third transistor's gate. Indeed, as I explained my opening declaration, a POSITA would understand this is *not* required at least because of the comma separating the functions of the third transistor and the CMVR circuit. *See* Flasck Decl. ¶¶ 93–95. In my opinion, the claim language is dispositive on this point. The phrase "during driving of [the] gate" appears twice in claim 1: (1) when referencing the third transistor and (2) when the OLED is in the "off" state." In both instances, it appears explicitly. But the phrase "during driving of the gate" does ***not*** appear in the portion of the claim describing the CMVR circuit:



1. A driving circuit for an image point of an image screen which has an organic light-emitting diode, comprising a capacitor; a feedback coupling; a first thin film transistor as a current-driving transistor for the diode; a second transistor which is connected by a current-conducting electrode with a gate of said first transistor and by a second current-conducting electrode with a data conductor and by its gate electrode with a scanning signal conductor; a third thin film transistor which during driving its gate through a driving conductor taps a diode driving current at an output of said first current-driving transistor and supplies a current measuring- and voltage regulating circuit, said current measuring- and voltage regulating circuit providing to the data conductor a voltage signal which is dependent on a current measuring result and a voltage comparison, so that the diode during driving of said gate of said third transistor due to its non-linear switching characteristic acts as a switch for a current deviation in said current measuring- and voltage regulating circuit.

10. A POSITA would understand that the portion of the claim highlighted in blue to be describing in a general way what the CMVR circuit does, possibly, but not necessarily during the time that the third transistor's gate is being driven. It is telling that the phrase "during driving of the gate" first appears to describe the third transistor and then is repeated to describe the diode, but does not appear to describe the CMVR circuit. Based on this claim language, a POSITA would understand the inventors did not intend to limit the claimed "providing" by the CMVR circuit's operation to only a period when the third transistor's gate is driven.

11. Further, in claim 1, the phrase "during driving of the gate" is always associated with an active verb: "taps," "supplies," and "acts." But in the portion of the claim describing the CMVR circuit, this phrase does not appear and the verb is the present participle "providing":



1. A driving circuit for an image point of an image screen which has an organic light-emitting diode, comprising a capacitor; a feedback coupling; a first thin film transistor as a current-driving transistor for the diode; a second transistor which is connected by a current-conducting electrode with a gate of said first transistor and by a second current-conducting electrode with a data conductor and by its gate electrode with a scanning signal conductor; a third thin film transistor which during driving its gate through a driving conductor taps a diode driving current at an output of said first current-driving transistor and supplies a current measuring- and voltage regulating circuit, said current measuring- and voltage regulating circuit providing to the data conductor a voltage signal which is dependent on a current measuring result and a voltage comparison, so that the diode during driving of said gate of said third transistor due to its non-linear switching characteristic acts as a switch for a current deviation in said current measuring- and voltage regulating circuit.

12. A POSITA would appreciate this difference and understand that the active verbs "taps," "supplies," and "acts" are required to occur driving of the gate but that the past participle "providing" is not required to occur during driving.

13. I disagree with Dr. Holberg's opinion that the '891 patent specification and figure support Defendants' proposed constructions. *See* Holberg Decl. ¶¶ 57–61. None of these disclosures say the claimed "providing" by the CMRV circuit must occur while the third transistor's gate is being driven, and a POSITA would not understand these disclosures in this way.

14. A POSITA would understand from the specification and figure that second transistor T2 and third transistor T3 can be turned on at different times. *See* '891 patent at 3:13–16 ("The gate of the transistor T3 in the shown embodiment is also connected with the scanning signal conductor A, as the gate of the transistor T2. However, it can be controlled by a separate drive conductor."). This is because T2 and T3 can be driven by different lines. If T2 and T3 were to always be driven simultaneously, there would be no reason to provide separate conductor lines.

15. A POSITA would therefore understand that the claim language, specification, and figure could cover modes of operation where the claimed "providing" by the CMVR circuit is performed whether or not the T3 gate is being driven. For example:

(1) Fast Closed Loop Mode. The current is measured rapidly, and corrected during one (each) write cycle. The CMVR circuit provides a corrected voltage to D to be put on capacitor C and the gate of transistor T1. During the initial test period (at the beginning of each write cycle) Both transistors T2 and T3 are turned on. The closed loop system brings the drive current to the correct level, and then T2 and T3 are simultaneously turned off.

(2) Storage Mode. Since the gates of transistors T2 and T3 can be driven independently, the entire matrix can be quickly calibrated, and the results stored for later use. In this matrix interrogation mode, T2 and T3 are not driven simultaneously. During at least some portion of the testing period, T3 will be turned on when T2 is turned off. During this period, it would make no sense for the CMVR circuit to send a voltage to line D, since this voltage would be blocked by T2 being turned off.

16. Regardless, Dr. Holberg does not identify any disclaimer in the specification and figure that requires the claimed "providing" by the CMVR circuit must necessarily occur only while the gate of transistor T3 is being driven. And certainly this is not required by the claim language for the reasons explained above and in my opening declaration.

B. "wherein all above mentioned elements of the driving circuit are located at a same side of said light emitting diode" ('891 patent claim 3)

Solas's Proposed Construction	Defendants' Proposed Construction
wherein all above mentioned elements of the driving circuit are electrically connected to and physically located on the same side of the layers of said light emitting diode	wherein all above mentioned elements of the driving circuit are electrically connected to the anode or cathode of said light emitting diode

17. Dr. Holberg's opinions for this "located at a same side" term miss the point. The parties agree that the term includes electrical connection. The only dispute is whether the term also refers to the physical location of the driving circuit elements. On this point, Dr. Holberg cannot reasonably dispute that the plain meaning of "located on the same side of said light emitting diode" includes some sense of physical location. That is how a POSITA would understand this claim

language in view of the intrinsic evidence. *See* Flasck Decl. ¶¶ 102–06. Nor does Dr. Holberg identify any clear disclaimer or lexicography that would exclude physical location. *See id.* ¶¶ 107–08. For example, the Applicant never redefined "located" to mean "electrically connected to," as required by Defendants' construction. Thus, Defendants' construction is incorrect and Solas's construction should be adopted.

18. The intrinsic evidence makes clear that "located on a same side" means physically located on the same side of the layers of the diode. For example, the claims and specification teach that the purpose of having the driving circuit elements "located on the same side" is to avoid any physical requirement to make vias or contract holes in the OLED organic layers. *See* '891 cl. 1; 4:41–45, 1:45–50. Further, the specification emphasizes that by locating "all circuit parts at one side of the LED element . . . ***a conventional layer sequence can be used during the manufacture***." *Id.* at 2:28–30 (emphasis added). These references to a "conventional layer sequence" and "during manufacture" clearly indicate to a POSITA that the term is describing the physical location of elements relative to layers of the diode.

19. Thus, the patent and the claim term is addressing a fundamentally physical issue. Cutting through holes or vias in the OLED layer stack (e.g., using photolithography) are problems of manufacturing and product yield. This is about physical structures, not only about which way current flows in a diode. Dr. Holberg improperly and unnecessarily conflates the concepts of electrical connection and physical location. *See* Holberg Decl. ¶¶ 62–64.

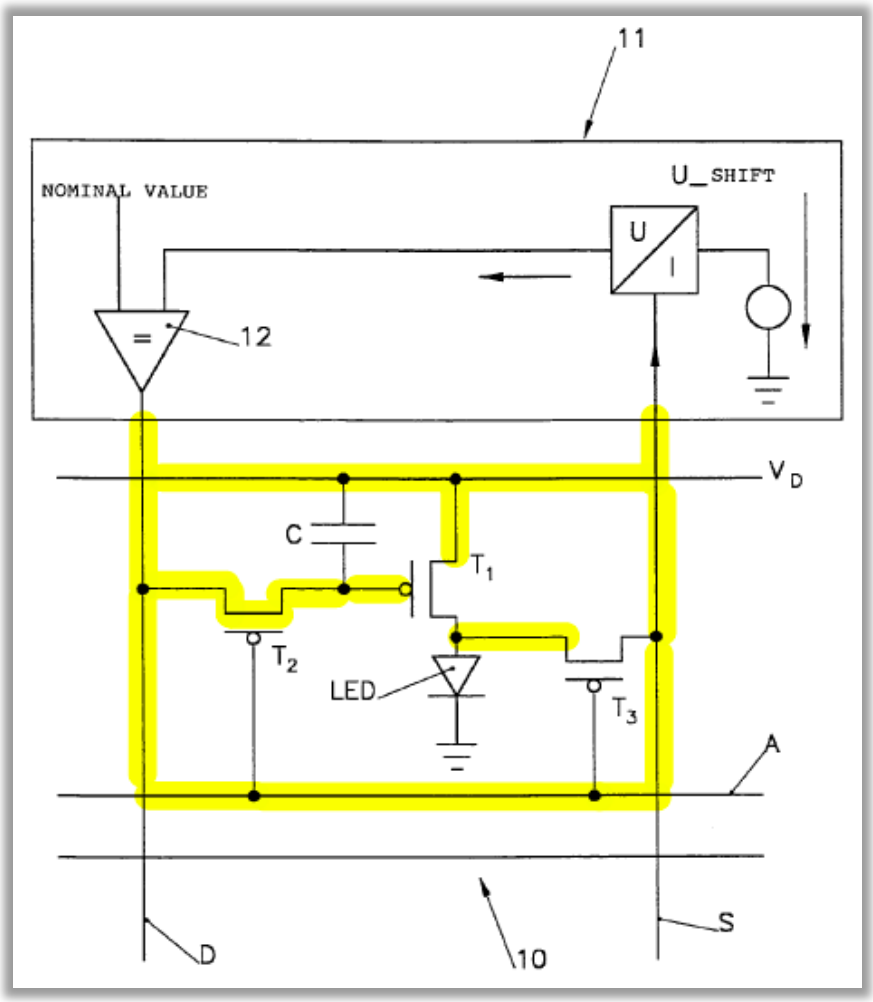
20. The claim term is part of a longer limitation that recites: "wherein all above mentioned elements of the driving circuit are located at a same side of said light emitting diode, *so that no contacts must be guided through a semiconductor material of the diode.*" *See* '891 patent, cl. 1. For short, I will refer to refer the italicized language as "no through holes." The no through holes

conduction supports Solas's construction, which requires the circuit elements to electrically connected to and physically located on the same side of the diode. Consider the four scenarios depending on whether the circuit elements are (a) physically located on or (b) electrically connected to, the same side of the diode:

P1E1	The circuit elements are physically located on and electrically connected to one side of the diode.
P1E2	The circuit elements are physically located on one side of the diode, but electrically connected to both sides of the diode.
P2E1	The circuit elements are physically located on both sides of the diode, but electrically connected to one side of the diode.
P2E2	The circuit elements are physically located on and electrically connected to both sides of the diode.

21. Solas's construction is scenario P1E1. This is the only scenario where the condition of "no through holes" can be met. Because the circuity is physically on one side and all circuit electrical connections go to only one OLED electrode, there is no need to form a through hole through the OLED layer of the diode.

22. In contrast, Defendants' construction includes scenario P2E1. In this scenario, the circuit elements are electrically connected to one side of the diode but physically located on both sides of the diode. Importantly, in this scenario, the circuit elements would still be electrically connected to each other. This is illustrated by the '891 patent figure, which depicts connections between the claimed "all above mentioned elements of the driving circuit" (e.g., capacitor, feedback coupling, three transistors, and CMVR circuit):



23. Because the circuit elements are physically located on both sides of the diode, a through hole through the OLED layer must exist to electrically connect a portion of the circuity on one side of the diode with a portion of the circuity on the other side of the diode. This is true even if the circuit elements only connects with one OLED electrode. Therefore, scenario P1E2 violates the "no through holes" condition.

24. Scenarios P1E2 and P2E2 also violate this condition. In P1E2, all circuitry is physically on one side but electrically connected to both sides of the diode. In this scenario, because conduct must be made to both OLED electrodes, a through hole must exist. In P2E2, the circuit elements are located on and electrically connected to both sides of the diode. In this scenario, portions of

the circuit on one physical side can connect to the OLED electrode on that physical side, while the portions of the circuitry on the second physical side can connect to the OLED electrode on that second physical side. But the two portions of circuitry (on opposite physical sides) must connect to each other. Therefore a through hole must exist. There is also the possibility with scenario PE2E2 that each or both of the circuit portions connect to each or both electrodes of the OLED. But even under these possibilities, a through hole must exist.

25. Based on the analysis above, the only condition which allows no through holes is P1E1. Or at least a POSITA would understand that that it is the condition most consistent with the no through holes condition. Therefore, for no through holes to exist, all portions of the drive circuit must be both (a) physically be on one side of the diode ***and*** (b) must electrically connected to that side. To avoid the necessity of a through hole the drive circuitry must be on the same side of the OLED *both physically and electrically*. Solas's proposed construction is correct.

26. I have reviewed the prosecution history of the '891 patent, including the portions relied on by Dr. Holberg, and disagree that there is any disclaimer or lexicography. *See* Holberg Decl. ¶¶ 65–68. For example, the Applicant explained during prosecution that claim 3 "is not ***just about*** the physical layers, but about the circuit elements." '891 FH at 152–53. This means that the limitation is about *both* physical layering and electrical connections—not "just" about the physical layers. Nor does the Applicant's statement that the limitation is "clearly shown in the drawings" operate as a disclaimer. In the same Office Action, the Applicant noted that the "interrelations between a circuit structure and a physically layering are trivial[.]" *Id.* at 153–54. A POSITA would view the circuit diagram in view of the '891 patent claims and specification, which teach that locating the circuit elements on the same side of the diode is to avoid the necessity of having through holes through the OLED layer and to address problems of manufacturing and product

yield. Thus, the circuit diagram, in context, informs a POSITA that the circuit elements would be physically located on the same side of the diode

IV. DISPUTED TERMS FOR '068 PATENT

A. "formed on said plurality of supply lines along said plurality of supply lines" ('068 patent claim 1)

"connected to said plurality of supply lines along said plurality of supply lines" ('068 patent claim 13)

Term	Solas's Proposed Construction	Defendants' Proposed Construction
"formed on said plurality of supply lines along said plurality of supply lines"	formed on said plurality of supply lines over the length or direction of said plurality of supply lines	formed on said plurality of supply lines over the length of said plurality of supply lines
"connected to said plurality of supply lines along said plurality of supply lines"	connected to said plurality of supply lines over the length or direction of said plurality of supply lines	connected to said plurality of supply lines over the length of said plurality of supply lines

27. Dr. Holberg's declaration improperly conflates the two limitations and ignores important elements of context in both cases. The claim clearly refers to a plurality (a group of more than one) of feed interconnectionss and to a plurality (a group of more than one) of supply lines. The claim language does not place conditions, restrictions, or limitations on individual feed interconnects or individual supply lines.

28. As Dr. Holberg acknowledges, the patent discloses two relevant embodiments. The first embodiment is shown here:

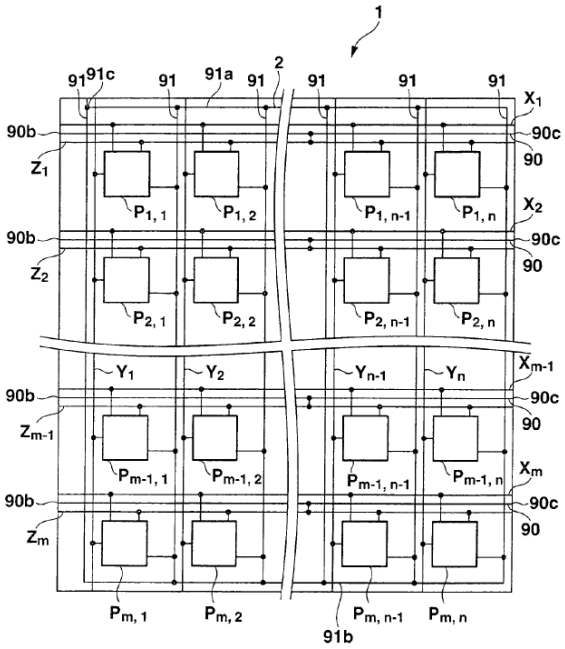


FIG.1

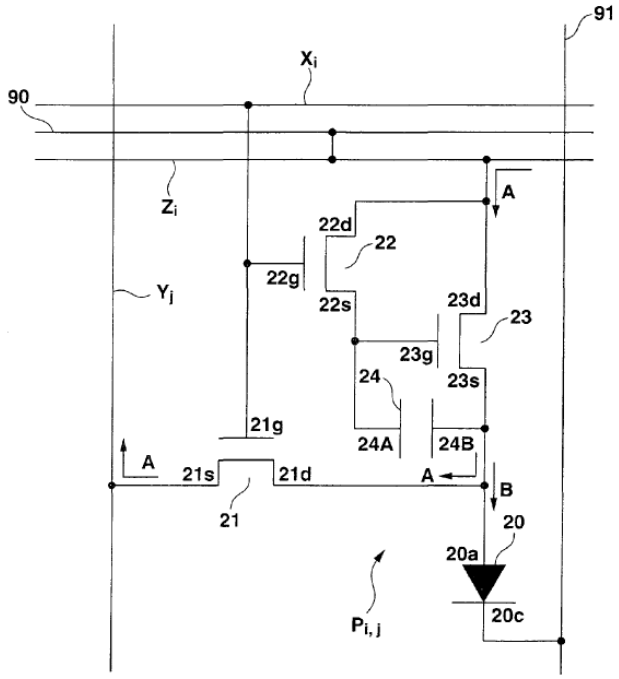


FIG.2

29. In this first embodiment, the each feed interconnections 90 runs parallel to and is connected to one of the supply lines (Zi). In fact, Fig 8 shows the feed interconnections formed directly on the top surface of the supply line Zi.

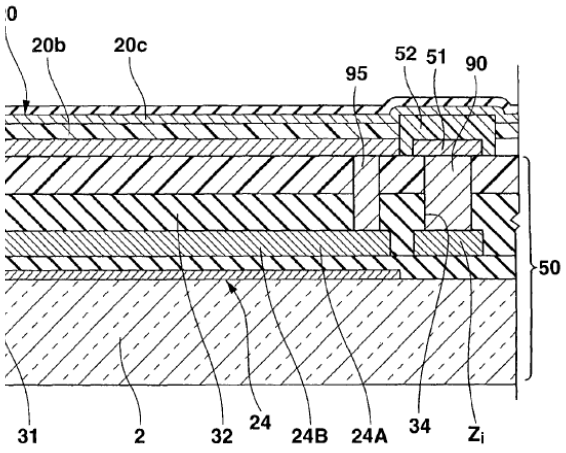


FIG.8

30. The second embodiment is shown below:

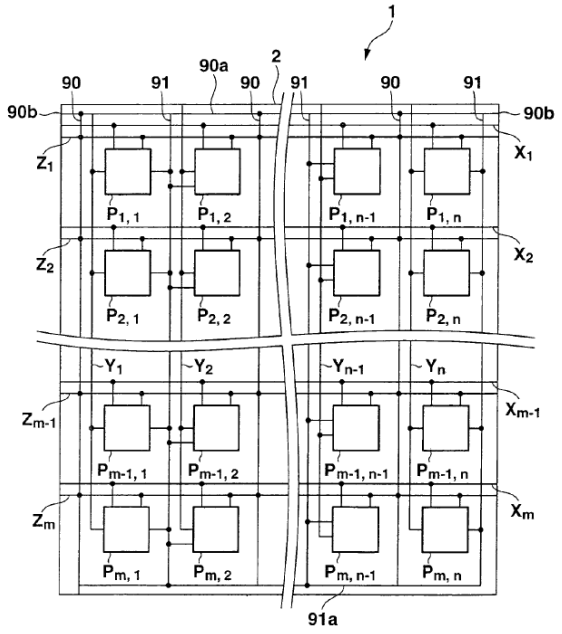


FIG.20

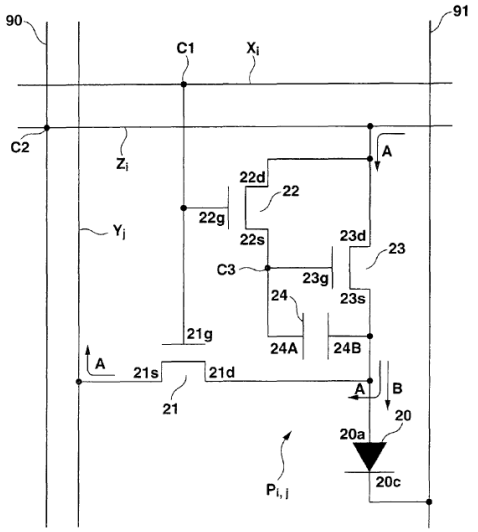


FIG.21

31. In this second embodiment, each feed interconnection 90 crosses and connects to each supply line (Zi) at the crossovers C2.

32. In this embodiment each feed interconnect runs along the plurality of supply lines at right angles. Therefore, the plurality of feed interconnects connects to and runs along the plurality of supply lines. The claim language is not referring to individual interconnections or lines. The claim language refers to pluralities.

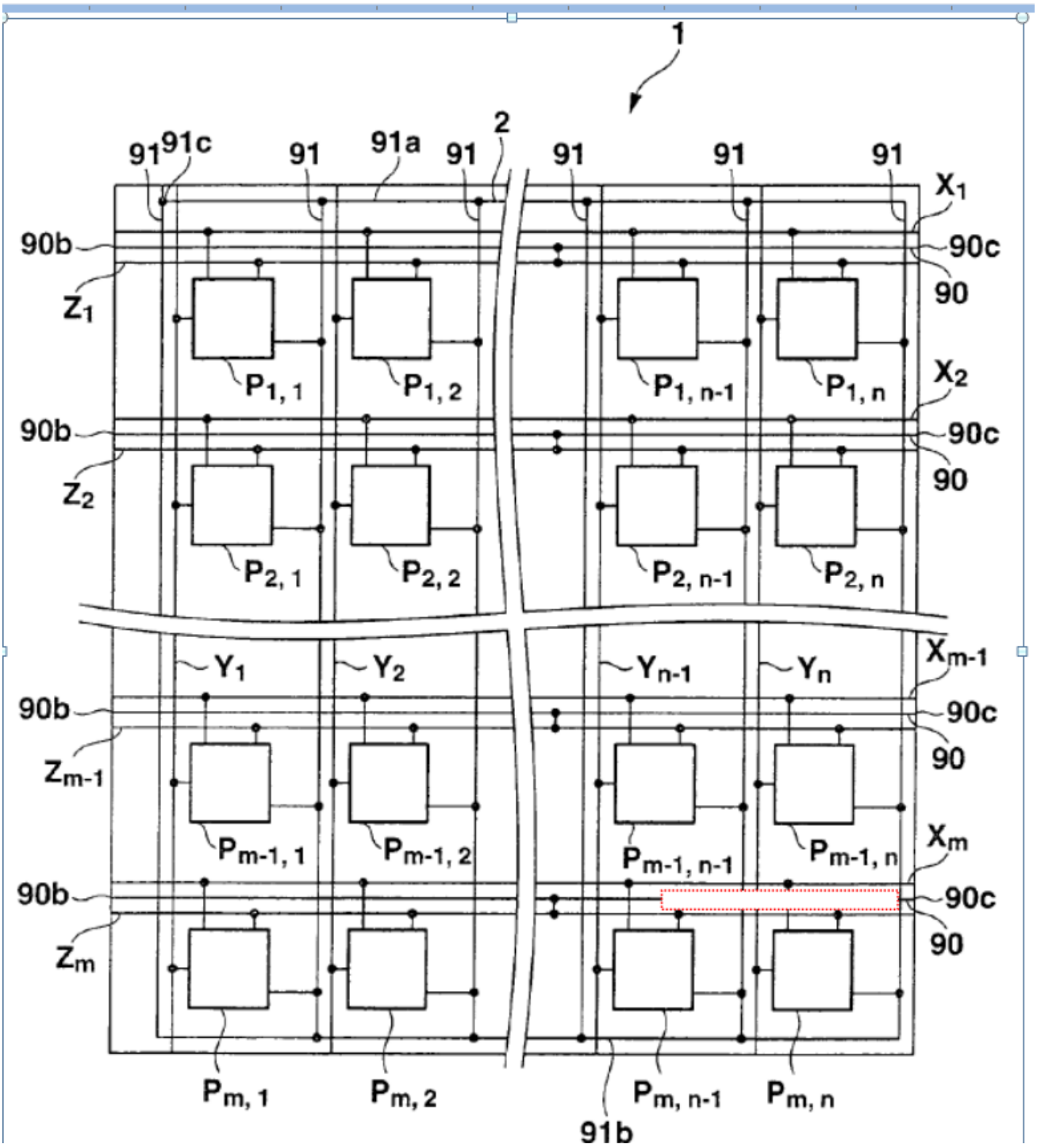
33. Both embodiments comport with the claim language in both claim 1 and claim 13. A POSITA would understand this.

34. The Defendants appear to interpret their own construction as requiring forming or connection over the ***entire*** length of the plurality of supply lines. A POSITA would not understand this to be a requirement of the claims or of the invention that is described in the patent.

35. Further, the patent describes the voltage drop problems mitigated by this aspect of the invention at 2:9-22, 2:39-41, 3:64-4:3, and 20:12-19. In any circuit there will be a voltage drop

across an element equal to the resistance times the current. The more high conductance feed interconnects mitigate voltage drops that would occur with thinner, higher resistance supply lines that would be required to run the full width of a display (several thousand pixels). It is true, however, that the feed interconnects do not need to run the full length of the supply lines to mitigate the voltage drop problem. A POSITA would know this.

36. Consider a case (shown annotated figure below) where the feed interconnection 90 stops short of the last two pixels in the bottom row right. In the worst case here (where the feed interconnection is formed directly over the supply line, the current for the final pixel would have to flow through not one but two pixel length supply lines. Although there would be some minor incremental voltage drop associated with the current traversing two lengths of pixel length supply lines instead of one, that voltage drop would be insignificant in most cases. So even in this case, the feed interconnection need not run along the entire length of the supply line to provide some mitigation of the IR voltage drop.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2
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90b
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Z_1
Z_2
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$P_{m,1}$
$P_{m,2}$
$P_{m,n-1}$
$P_{m,n}$
91b

B. "patterned" ('068 patent claims 1, 13)

Solas's Proposed Construction	Defendants' Proposed Construction
formed in one or more layers	formed in a single layer

37. Dr. Holberg does not separately address the term "patterned" but instead combines his opinions for "patterned" and "patterned together." *See* Holberg Decl. ¶¶ 89–115. Thus, I respond to his opinions for both terms under the "patterned together" term below.

38. But I note that Dr. Holberg makes an important admission in his opinions. He opines that "it's clear to a POSITA that the '068 patent uses 'patterned' to describe the formation of the display panel layer by layer, consistent with its ordinary usage in the art." Holberg Dec. ¶ 114. This supports the opinions in my opening declaration that "patterned" is a known term of art with a plain meaning to a POSITA. *See* Flasck Decl. ¶ 117. It also supports my opinion that the '068 patent uses "patterned" consistent with its plain and ordinary meaning. *See id.* ¶ 118.

39. Dr. Holberg's statement also supports Solas's proposed construction of "formed in one or more layers" and undermines Defendants' proposed construction of "formed in a single layer." In particular, Dr. Holberg's statement that "patterned" refers to the "formation of the display panel layer by layer" implies that "patterning" can be applied to a single layer or to multiple layers, such as a stack. *See id.* ¶ 117. The phrase "layer by layer" implies that the structure being formed can be a single or multiple layers. Indeed, if "patterned" were restricted to being formed in a single layer (under Defendants' proposed construction) it would not make sense to describe that single layer as being formed layer by layer. Thus, Dr. Holberg's statement contradicts Defendants' proposed construction of "formed in a single layer." Nor does Dr. Holberg identify any disclaimer or lexicography that supports such extreme narrowing.

C. "patterned together" ('068 patent claims 1, 13)

Solas's Proposed Construction	Defendants' Proposed Construction
patterned to fit together	patterned at the same time

40. Dr. Holberg opines that the term "patterned together" should be construed as "patterned at the same time." *See* Holberg Decl. ¶¶ 92, 114. This proposed construction repeats the claim term "patterned." Thus, Dr. Holberg (and Defendants') construction is that "together" means "at the same time." By using "at the same time," this construction imposes a strict requirement of temporal simultaneity. This requirement is unjustified and contradicted by the '068 patent.

41. As discussed in my opening declaration, the plain and ordinary meaning of "together" does not require temporal simultaneity or even close temporal proximity. *See* Flasck Decl. ¶¶ 120–25. A POSITA would understand that in the context of the '068 patent, elements are "patterned together" if they are in close spatial proximity and designed to fit together in the display panel. *See id.* This understanding is reflected in the '722 patent discussed in my opening declaration. In the '722 patent elements **294** and **298** have different functions and fill patterns. A POSITA would therefore understand that they **294** and **298** require different materials and are different material layers. Further, **294** and **298** are not stacked on each other. Therefore they were deposited at different times; they are not the same layer. Yet, the '772 patent states that **294** and **298** are "patterned together." This makes Dr. Holberg's "formed at the same time from a single layer" construction untenable. Instead, in the '722 patent, **294** and **298** are formed to spatially conform to each other's shape. This is consistent with and further supports Solas's construction.

42. Further, the teachings of the '068 patent contradict Defendants' construction. In the patent, the supply lines are "patterned together" with the sources and drains of the driving transistors. '068 patent at cls. 1, 13; 2:52–53, 3:39–59. And in the patent, the scan lines are "patterned together"

with the sources and drains. *Id.* at cl. 14, 2:61–65 ("Preferably, a substrate according to claim **1,** further comprising a plurality of scan lines which are patterned together with the sources and drains of the plurality of driving transistors and arrayed to cross the plurality of supply lines via the gate insulating film."), 3:39–59.

43. Thus, the patent teaches that the supply lines, the scan lines and the transistor sources and drain were all "patterned together." The patent further teaches that the scan lines cross the supply lines via the gate insulating film. *Id.* at 2:62–65, 3:39–59. Therefore, at the cross-overs, the scan line is above the gate insulator and the gate insulator is above the supply line. Therefore, in my opinion, the supply line layer was patterned before the gate oxide layer was patterned, and the gate oxide layer was patterned before the scan line layer was patterned.

44. In sum, in the patent's preferred embodiment, the scan lines and the supply lines are both (a) "patterned together" and (b) not patterned at the same time. The scan line layer and the supply line layer are each distinct and separate layers. Therefore, in my opinion, "patterned together" cannot mean "patterned at the same time." Furthermore, "patterned" cannot mean "formed of the same layer" or "formed in a single layer." Dr. Holberg is simply wrong in his constructions for both "patterned" and" patterned together." These constructions are inconsistent with the '068 specification, and would exclude preferred embodiments. I understand that constructions that would exclude embodiments are rarely, if ever, correct.

45. In contrast, the preferred embodiment is consistent with Solas's construction. The scan lines and supply lines are in close spatial proximity and designed to fit together in the display panel. This supports Solas's construction of "patterned together" as "patterned to fit together." Solas's construction is correct and should be adopted.

D. "feed interconnections" ('068 patent claims 1, 10, 12, 13, 17)

Solas's Proposed Construction	Defendants' Proposed Construction
conductive structures in a layer or layers that provide connections to a source that supplies voltage and/or current	conductive structures in a layer or layers different from the gates, sources and drains that provide connections to a source that supplies voltage and/or current

46. I disagree with Dr. Holberg's opinion that a POSITA would understand the term "feed interconnections" to require that they be formed in layers that do not overlap with any of the layers used to form the gates, sources and drains. I also see nothing in the specification that teaches this is a requirement of the invention.

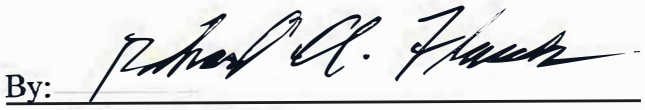
47. For example, the summary of the invention section of the specification describes four "aspects" of the invention. (4:16.) The summary only mentions forming feed interconnections separately in its discussion of one of those aspects. (3:60–64.) That suggests that a POSITA would understand that forming feed interconnections separately is not a mandatory feature of the invention.

48. Dr. Holberg argues that forming feed interconnections from layers different from the gates, sources, and drains is important because the specification describes suppressing voltage drop and signal delay as an object of the invention. But, he does not explain why that object could not be achieved by feed interconnections that do share layers with one or more of the gates, sources, and drains, and a POSITA would not understand that separately formed feed interconnections are necessary to achieve this object.

V. CONCLUSION

I declare under penalty of perjury that the foregoing is true and correct.

Executed April 3, 2020, in San Ramon, California.

By: 

Richard A. Flasck